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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,239	WHITTAKER, EDWARD J.W.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, and 4-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-17* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Drawings

The amendment and drawings submitted on Dec 12, 2005 have been reviewed and considered with the following results:

The replacement sheets, and/or amended changes to the disclosure, overcame most of the objections to the drawings as described within the previous Office Action, which have now been withdrawn. However, since "Q3" remains within Fig. 3, that drawing objection is maintained. Therefore, the replacement sheets submitted on Dec 12th have not been approved. Also, due to some of the changes made within the amendment/drawings, the figures and disclosure were carefully reviewed, and other objections to the drawings were noted. These are also described later under the appropriate section, along with the "Q3" related objection.

Although the new abstract overcame most of the objections described with respect to the original abstract, the present abstract still contains the term "novel." Also, the abstract now contains a merit related phrase. Therefore, the previous objections to the original abstract have now been withdrawn, but new objections are described later with respect to the new abstract.

The amended paragraphs, or changes to the figures, overcame many of the objections to the disclosure as described in the previous Office Action. However, some of the objections were not addressed, or addressed satisfactorily. For example, the objections to some paragraphs (e.g. 0024, 0034, 0035, and 0038) with respect to the current mirror ports still need work; the "are used in order" phrase of paragraph 0030 was not addressed; and the wrong "first and second" phrase in paragraph 0039 was changed. Therefore, those objections have been maintained, and/or modified with respect to some associated amended change, and are described later under the

appropriate section. All the other objections to the disclosure described in the previous Office Action have been withdrawn. However, various other concerns were also noted when the original disclosure, and amended paragraphs, were carefully reviewed. These are also described later under the appropriate section.

The cancellation of claims 3 and 18-20 rendered their respective objections, and/or rejections, moot.

The phrase "Claims 1, 2, 4-8, 9, 2, 13, and 14 have been amended" on page 15 of the amendment is misleading, or inaccurate. The Dec 12th amendment does not show any change made to claims 9, 13 and 14, which are clearly identified as "(original)", wherein claims 10 and 16 have actually been amended, but these two claims are not mentioned on the page 15 phrase. Therefore, it is not known if amended changes to claims 9, 13, and 14 were meant to be made, but were overlooked.

The amended changes to claims 2, 5, 7, 10, and 16 overcame most of the objections to claims 1-2, and 4-17 described in the previous Office Action. However, the objections to claims 8-9, and the claims they depend upon, with respect to the use of --further--, have been maintained. Therefore, all of the other claim objections described in the previous Office Action have now been withdrawn, but those related to claims 8-10 have been maintained. These are described later under the appropriate section, and associated comments are described later under the Response to Arguments/Comments section. Also, an overlooked objection to claim 1 was noted when the claims were reconsidered. This objection is also described later under the appropriate section.

The amended claims overcame some of the rejections of claims 1-2, and 4-17 under 35 U.S.C. 112 as described in the previous Office Action, and those rejections have been withdrawn. However, the rejections of claims 7 (i.e. "third"), 8 (i.e. "second"), 11 (i.e. "second"), and 13 (i.e. "source" and "second") have not been addressed/corrected. Also, amended claim 8 created a new problem. Therefore, these known rejections are described later under the appropriate section.

The amended claims overcame all the prior art rejections described in the previous Office Action. Therefore, the following rejections have been withdrawn: 1) 1-2, and 8 under 35 U.S.C. 102(b), with respect to Min; 2) claims 1-2, and 8-10 under 35 U.S.C. 102(e), with respect to Aude et al.; and 3) claims 4-7, and 13 under 35 U.S.C. 103(a) with respect to Aude et al. The reference of Min lacks the first/second bipolar transistors, and it clearly discloses the areas of the MOS transistors shown have equal areas. Therefore, there is no motivation to replace at least transistors MN10 and MN5 with bipolar transistors, and to ensure at least the current mirror circuit, or the first/second bipolar transistors, provide a current N or M times their respective input current, wherein at least N or M is not equal to one (e.g. output current ≠input current) as understood from the added limitations now recited within independent claim 1. The Aude et al. reference does not show the base terminals of first/second bipolar transistors X1/X2 coupled together as now recited within claim 1, and there is no strong motivation to make that type of connection.

However, several other references were found during a recent update search, and at least some of these read on at least the basic limitations recited within at least independent claim 1 as

now amended. Therefore, these prior art rejections are described later under the appropriate section.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Fig. 2 lacks "200a", which is identified in paragraphs 0017 (line 5), 0018 (line 3), and 0019 (lines 3-4, 6, and 14-15). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because "NI M_{in}" in Fig. 2 should be corrected to ensure the "I" and "$_{in}$" portions are together (i.e. as -- I_{in}--) to minimize possible confusion with respect to what "M_{in}" means within the present labeling. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and

where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are also objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "Q3" of Fig. 3 is not disclosed, and since "Q1" and "Q2" are clearly shown, and disclosed, as transistors, it is suggested "Q3" be completely removed from Fig. 3 to minimize possible confusion (e.g. that it corresponds with some transistor). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The applicant is reminded of the proper content of an abstract of the disclosure.

The replacement abstract (i.e. on page 13 of the Dec 12th amendment) of the disclosure is objected to because the abstract should avoid using phrasing which can be implied, and it should not refer to purported merits or speculative applications of the invention. In this case, it is suggested the phrase "The novel circuit provides significant improvements in precision" on lines 4-5 be changed to --The circuit provides precision--. This type of change will remove: 1) the implied "novel" term (i.e. the abstract is understood to be a summarized description of an invention, which by itself should be new, or "novel", since an application should not be submitted for an old, or known, invention); and 2) the phrase "significant improvements" which is describes purported merits. Therefore, correction is required. See MPEP § 608.01(b).

Due to some amended changes to the disclosure that created some new concerns, the original disclosure and amended paragraphs were carefully reviewed and considered. The disclosure is objected to because of the following informalities: Page 2, line 6 of paragraph 0005 "termThey" should be changed to --term. They-- to remove the run on words and sentences. On amended paragraph 0020, line 12, it is suggested "resistor, R1," be changed to --resistor 231-- since "R1" is not shown in Fig. 2, and this change will then be consistent with related changes to paragraphs 0017, 0019, and 0022. The change to line 2 of amended paragraph 0024 creates new problems. Using the applicant's own Fig 3 as a reference, it is believed the "first portion" being described refers to transistor Q1 201, which is disposed between port 305b and second supply voltage port 300b. However, "305b" is the "second current mirror port", wherein "305a" is the "first current mirror port" (i.e. see the last three lines of paragraph 0023). Therefore, to maintain

consistent labeling throughout the disclosure, it is suggested "the first current mirror port 305a" on line 2 of the amended paragraph 0024 be changed to --the second current mirror port 305b--, and "the second current mirror port 305a" on line 10 of the same paragraph be changed to --the first current mirror port 305a--. Line 7 of amended paragraph 0025 should have "capacitor" capitalized since it starts a new sentence. Amended paragraph 0026, line 2 should have --its-- added prior to "gate" to improve word flow, and both occurrences of "C1" on line 3 should be deleted to correspond to similar changes made within paragraph 0025, and because Fig. 3 does not show a "C1" designator. Original paragraph 0027, line 5 should have --second current mirror-- instead of "first current mirror"; and "R1" on line 12 should be deleted since Fig. 3 does not show that designator. Original paragraph 0028 should have "C1" deleted from lines 10 and 14 for reasons similar to previous descriptions. To improve word flow, and also minimize possible confusion with respect to the phrasing that implies PNP transistors are already shown, it is suggested "the PNP transistors are used in order to replace" be replaced with --PNP transistors can be used instead of--. Since "first portion" on line 2 of amended paragraph 0034 was changed to "second portion", the following changes are suggested to help maintain consistent labeling throughout the paragraphs, and correspond to the circuit structure shown within the figures: 1) paragraph 0034, "second portion" on lines 3 and 4 should be changed to --first portion--; and 2) amended paragraph 0035, line 8 "first current" should be --second current-- (e.g. see lines 10-11 of paragraph 0034, and line 2 of paragraph 0036), and line 9 "second current" should be --first current-- (e.g. see line 2 of paragraph 0034). It is suggested --its-- be added prior to "gate" on line 2 of amended paragraph 0037 to improve word flow. Amended paragraph 0038, line 5 "second current" should be --first current-- (e.g. see line 2 of paragraph 0034). Amended

paragraph 0039, line 6 should have "seventh and sixth" returned to the original phrasing --First and second--, and line 7 should have "first and second bipolar" changed to --seventh and sixth bipolar-- to correct an inadvertent oversight (i.e. amended change was made to incorrect line). Appropriate corrections are required. However, it is suggested that when changes are made, they should be verified for consistent use throughout the disclosure, and with respect to what is shown within the figures. This will help to minimize possible confusion, and/or misleading type descriptions.

Claim Objections

Claims 1-2, and 4-17 are objected to because of the following informalities: Claim 1, line 6 should have "supply port" changed to --supply voltage port-- to ensure consistent labeling throughout the claims. Since claim 1 already cites the "current mirror circuit" comprises "a first current mirror port and a second current mirror port" on line 4, it is strongly suggested that "the current mirror circuit comprises" within the preambles of both claims 8 and 9 have either the term --further-- or --also-- added prior to "comprises." Such a change would clearly indicate the limitations within claims 8 and 9 are in addition to at least one related element within the circuit as cited in any claim(s) upon which they depend. Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants

regards as the invention. The use of "third field effect transistor", "third gate terminal", "third drain terminal", and third source terminal" within claim 7 imply first and second FETs, gate terminals, drain terminals, and source terminals have been previously identified within the claim's chain of dependency. Therefore, claim 7 is indefinite since it is not clear if claim 7 was meant to depend on claim 9, which identifies the first/second FETs, etc. within its chain of dependency. For similar reasons, the use of "second FET", "second gate terminal", "second drain terminal", and "second source terminal" within claim 8 imply a first FET, gate terminal, drain terminal, and source terminal have been previously identified within the claim's chain of dependency. It is not understood what the phrasing "second FET one of coupled to and resistively coupled to the first base terminal" actually means on lines 5-6 of claim 8. The use of "second current source" in claim 11 implies a first current source that has not been clearly identified within the claim's chain of dependency. Although claim 2 does recite "a current sink", that is not automatically considered a "current source" since some references indicate a current source supplies current from a higher potential (e.g. Vcc) to increase potential at some point (e.g. a node), wherein a current sink sinks current from the same point to decrease potential at that point. Therefore, do the applicants' mean to consider the "current sink" of claim 2 as a first current source? The phrase "between the third source and third gate terminals" on line 2 of claim 13 is misleading and/or inaccurate. For example, was --drain-- meant instead of "source" (e.g. see capacitor 341 and transistor 313 in the applicant's Fig. 3)? The use of "a second resistor" in claim 13, line 4 implies a first resistor that has not been clearly identified within the claim's chain of dependency.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-5, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akioka et al. (Akioka), a reference considered during the recent update search. Fig. 4 shows a circuit comprising first supply voltage port VCC; second supply voltage port VEE; current mirror circuit M1,M2,M5 comprising a first current mirror port (i.e. the unlabeled node between M2 and Q3) and a second current mirror port (i.e. the unlabeled node between M1 and Q2), wherein one of ordinary skill in the art would understand an input current is propagated from the first supply voltage port to second supply voltage port VEE through current mirror circuit M1, M2,M5 with the first current mirror port providing N times the input current; and current ratioing circuit Q3,Q11,Q20-Q21,R20-R21 comprising first portion Q3 between the first current mirror port and second supply voltage port VEE, second portion Q11,Q20-Q21,R20-R21 between first supply voltage port VCC and second supply voltage port VEE, with the current ratioing circuit propagating M times N times the input current through load current path Q20-Q21,R20-R21 of the second portion. First portion Q3 comprises first bipolar transistor Q3 having a first base terminal and a first collector terminal coupled with the first current mirror port, and a first emitter terminal coupled to second supply voltage port VEE. Second portion Q11,Q20-Q21,R20-R21 comprises second bipolar transistor Q11 having a second base terminal coupled to the first base terminal, a second collector terminal coupled to load current path Q20-Q21,R20-

R21, and a second emitter terminal coupled to second supply voltage port VEE. One of ordinary skill in the art would understand that second bipolar transistor Q11 is M times larger than first bipolar transistor Q3. Although the reference does not clearly show or disclose what the ratio (e.g. N or M) between the transistors actually are, or the use of plural transistors coupled in parallel, Akioka does disclose some relationships between associated transistors within current mirror type circuits (e.g. see column 7, lies 42-55, and column 10, lines 63-66). Also, one of ordinary skill in the art would understand that one transistor within a current mirror type circuit is X times another transistor within the same current mirror type circuit, wherein X can be a positive number larger than, less than, or equal to one. Therefore, it would have been obvious to one of ordinary skill in the art to have at least one of N (i.e. associated with the ratio of transistors within current mirror circuit M1,M2,M5) and M (i.e. associated with the ratio of first/second transistors Q3/Q11 within the current ratioing circuit Q3,Q11,Q20-Q21,R20,R21). Unless current I4 through second bipolar transistor Q11 is to be equal to current I2 through M1, one of ordinary skill in the art would understand at least one of N and M is other than 1, thus claim 1 is rendered obvious. With at least one of N and M other than 1, current I4 can be made a multiple greater than the input current, or a fraction (e.g. another type of multiple) of the input current. [Note: Due to the current mirror structure of transistors M1,M2,M5, and of transistors Q3,Q11, one of ordinary skill in the art would know the ratio between the transistors within the current mirror structure would determine how the input and output currents of each respective current mirror structure would relate to one another. For example, if M1 is twice the size of M2, the current flowing through M2 would be 0.5 times the current flowing through M1, but if M2 is twice the size of M1, the current flowing through M2 would be 2 times the current flowing

through M1, and current I4 through Q11 would be proportional to the current flowing through series coupled M2 and Q3.] Transistor Q2 and resistor R2 comprise a current sink coupled between second supply voltage port VEE and the second current mirror port for sinking the input current through the current mirror circuit M1,M2,M5 from the second current mirror port to second supply voltage port VEE, rendering claim 2 obvious. It would have been obvious to one of ordinary skill in the art to have each of N and M other than 1. This renders claim 4 obvious. By having both N and M other than 1, the desired amount of current I4 flowing through second bipolar transistor Q11 could be selected to be a multiple of the input current, especially if a much larger current is required with respect to the input current. It also would have been obvious to one of ordinary skill in the art to replace the single second bipolar transistor Q11 with a plurality of bipolar transistors coupled in parallel, wherein the number of transistors in parallel would be M times first bipolar transistor Q3, thus rendering claim 5 obvious. For example, if the output current of a current mirror structure was required to be 5 times the input current, the output transistor could be a single transistor that is 5 times the size of the corresponding input transistor, or the output transistor could comprise 5 single transistors coupled in parallel, wherein each transistor would have the same size of the corresponding input transistor. Whether a single transistor, or a plurality of parallel coupled transistors, would be used would depend on the desired output current, and how much area was available for the overall circuit. Current mirror circuit M1,M2,M5 comprises second FET M2 with a second gate terminal, and the second source and second drain terminals disposed in series between first supply voltage port VCC and the second current mirror port, wherein the second source of second FET M2 is effectively coupled to the first base terminal (of Q3) via the resistance within M2, thus claim 8 is rendered

obvious. Current mirror circuit M1,M2,M5 also comprises first FET M1 with a first gate terminal, and its first source and first drain terminals disposed in series between first supply voltage port VCC and the first current mirror port. The first gate terminal and the first drain terminal of first FET M1 are coupled together, and one of ordinary skill in the art would know that first FET M1 is N times (i.e. proportional) wider than second FET M2, thus claim 9 is also rendered obvious. First FET M1 and second FET M2 are PFETs (i.e. PMOS, p-channel, or P-type, FETs), rendering obvious claim 10.

No claim is allowable as presently written.

Claims 3 and 18-20 have been cancelled.

Allowable Subject Matter

However, claim 6 is only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the circuit also comprises a current path between the first supply voltage port and the coupled first/second base terminals as recited within claim 6.

Also, claims 7, and 11-17, would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Other than its rejection(s) under 35 U.S.C. 112, claim 7 depends on claim 6, which is only objected to as described above, and claims 13-14 and 16-17 depend on claim 7. Also, there is presently no strong motivation to modify or combine any prior art reference(s) to ensure the circuit comprises a second current

source coupled to the first/second base terminals as recited within claim 11, upon which claims 12 and 15 depend.

Prior Art

The other prior art reference cited on the accompanying PTO-892 is deemed relevant to at least some of the claimed invention. The reference of Tagami et al. was also found during the recent update search, and it shows a circuit in Fig. 3 comprising current mirror 10-11 (with a ratio (e.g. multiplication factor) disclosed on column 7, lines 24-27 with respect to associated Fig. 1), and current ratioing circuit portion 200 with first/second bipolar transistors 33/34, wherein current output terminal 32 is connected to a functional circuit as disclosed on column 10, lines 8-10. Although not used in any formal rejections described above, it would have been obvious to one of ordinary skill in the art to consider this functional circuit as a load current path which utilizes the current flowing through second bipolar transistor 34. Column 10, lines 34-35 disclose how currents Iin1 and Iout1 relate to one another when first/second bipolar transistors 33/34 are of the same size. However, one of ordinary skill in the art would also understand that if the transistors were not the same size, the input/output current relationships would not be equal to one another (i.e. having a 1:1 ratio), but they would still be proportional to one another (e.g. Iout1 through transistor 34 would be equal to M times Iin1 through transistor 33, wherein M is associated with the size of transistor 34 with respect to transistor 33). Therefore, this reference should also be carefully reviewed with respect to the present application's basic claimed limitations.

Response to Arguments/Comments

The applicants comments filed Dec 12, 2005 have been fully considered but they are not persuasive with respect to the examiner's suggested use of --further-- within claims 8 and 9. When a claim makes a statement such as "the current mirror circuit comprises", this phrasing implies it is the first limitation to clearly identify some type of element (e.g. transistor, resistor, node, etc) within that particular circuit. However, in the case of claims 8 and 9, the current mirror circuit already comprises "a first current mirror port and a second current mirror port" as cited on line 4 of claim 1. Therefore, it is strongly believed claims 8 and 9 should be amended to clearly indicate that the limitations recited within those claims are in addition to those already cited in claim 1.

The rejections described within the present Office Action, as well as within the previous Office Action, are deemed proper with respect to the broadest reasonable interpretation of the prior art record and the claimed limitations.

The applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry L. Englund

1 March 2006

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800